AMENDMENTS

In the Claims:

Please amend the claims as indicated hereafter.

1. (Previously Presented) An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:

circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;

a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set.

2. (Original) The apparatus of claim 1, wherein said sum value and said carry value are dual rail encoded values.

3-6. (Canceled)

7. (Previously Presented) A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:

receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;

logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and

providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set.

8. (Previously Presented) The method of claim 7, wherein said step of logically combining comprises adding the third propagate, kill, and generate representation and the carry-in value.

9. (Canceled)

10. (Previously Presented) The method of claim 7, wherein said step of logically combining further comprises generating dual rail encoded values.

11-22. (Canceled)

23. (Previously Presented) The apparatus of claim 1, wherein the sum value is a function of the third propagate representation and the carry-in value.

24. (Previously Presented) The apparatus of claim 23, wherein the sum value is the XOR combination of the third propagate representation and the carry-in value.

25. (Previously Presented) The apparatus of claim 1, wherein the carry value is a function of the third propagate representation, the carry-in value, and the third generate representation.

26. (Previously Presented) The apparatus of claim 25, wherein the carry value is the OR combination of the third generate representation with the AND combination of the third propagate representation and the carry-in value.

27. (Previously Presented) The apparatus of claim 1, wherein the carry-out value is a function of the first and second generate representations.

28. (Previously Presented) The apparatus of claim 27, wherein the carry-out value is the OR combination of the first and second generate representations.

29. (Previously Presented) The apparatus of claim 1, wherein the circuitry provides the sum value at a third output.

30. (Previously Presented) The method of claim 7, wherein said step of logically combining comprises a XOR combination of the third propagate representation and the carry-in value.

31. (Previously Presented) The method of claim 7, wherein said step of logically combining comprises an OR combination of the third generate representation with the AND combination of the third propagate representation and the carry-in value.

32. (Previously Presented) The method of claim 7, wherein said step of generating comprises an OR combination of the first and second generate representations.

33. (Previously Presented) The apparatus of claim 1, wherein only one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can simultaneously be at the particular binary value.

34. (Previously Presented) The apparatus of claim 1, wherein each set bit of the logical value has a binary value of one.

35. (Previously Presented) An apparatus for performing addition, said apparatus comprising:

circuitry configured to receive an operand defining a logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, wherein the logical value, when decoded into a non-PKG form, has a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that none of the bits of the logical value are set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two bits of the logical value are set; and

a carry save adder configured to add the operand in PKG form to a carry bit without decoding the operand from PKG form.

36. (Previously Presented) The apparatus of claim 35, wherein each set bit of the logical value has a binary value of one.

37. (New) The method of claim 7, wherein each set bit of the logical value has a binary value of one.